AMENDMENTS TO THE SPECIFICATION:

Please cancel the originally-filed Abstract of the Disclosure, and add the accompanying new Abstract of the Disclosure which appears on a separate sheet in the Appendix.

Please delete the heading "Description" beginning on page 1, line 1.

Please add the following new headings, paragraph and heading, after the title on line 4 of page 1:

--Description

Cross Reference to Related Applications

This is the 35 USC 371 national stage of international application PCT/DE2003/003524, filed on 23 October 2003, which designated the United States of America.

Field of the Invention—

Please add the following new heading after the paragraph ending on line 15 of page 1:

--Background of the Invention—

Please add the following new heading after the paragraph ending on line 11 of page 4:

--Summary of the Invention—

Please add the following new heading after the paragraph ending on line 5 of page 7:

--Brief Description of the Drawings--

Please add the following new heading after the paragraph ending on line 19 of page 7:

--Detailed Description of the Invention--

Please add the following new paragraph after the paragraph ending on line 23 of page 9:

-- In the "Journal of Systems Architecture", vol. 47, 2002, pages 1043 to 1064, the fundamental operation of reconfigurable models of FSMs and their implementation in FPGAs (Field Programmable Gate Arrays) as special PLDs is described. The design methods are considered in order to code applications for reconfigurable chips. The hardware used for this purpose, and thus the architecture of the chips, follow the state of the art; i.e. known architectures are used as a basis. However, no actual technical embodiments are demonstrated.--

Please add the following new paragraph after the paragraph ending on line 3 of page 14:

-- This extra PLD forms the configurable changeover logic block according to the invention. It must necessarily have access to the configuration section of the other logic blocks operating normally since it would otherwise not be possible to effect a reconfiguration. For this reason, the outputs of the logic changeover block must be connected at least partially to the code area of the (other) logic blocks to be configured so that these can be configured or it is possible to switch between their configurations. Such a "changeover" connection does not exist in known constructions and other non-changeover logic blocks do not have such connections either.--

Please add the following new paragraph after the paragraph ending on line 33 of page 15:

-- According to a corresponding actual exemplary embodiment, a traffic light system will be selected which has two modes, namely a day mode and a night mode. Each of these modes is designed as one FSM; normal implementation is then that both are

also really implemented on the PLD and thus need approximately twice the space.

The implementation in a reconfigurable architecture according to the invention then provides that both modes are implemented in the same part, in such a manner that one is active (e.g. day mode), whereas the other one (then: night mode) is only inactive in the memory. The changeover logic block then detects the changeover conditions such as time and/or darkness and/or traffic volume and/or any other external signal and, in dependence on this, initiates a changeover between the modes, e.g. by reloading the memory content. For this purpose, the changeover logic block must have access to the respective configuration memory of the other blocks.--